Workshop on

Energy-Aware COmputing (EACO)[1]

Beyond the State of the Art

Wednesday, 13th July 2011, 11:30 - 18:00
Thursday, 14th July 2011, 8:30 - 14:00

Room 0.01 in The Systems Centre, Ground Floor, Merchant Venturers Building, Woodland Road, Bristol BS8 1UB

Purpose: To bring together researchers and engineers with interests in *energy-aware computing* for discussions to identify intellectual challenges that can be developed into collaborative research projects. We strive to go significantly beyond the state of the art.

Agenda

Wednesday, 13th July 2011

11:30 **Registration**
12:00 **Welcome and Introduction** - Kerstin Eder and David May, University of Bristol
12:30 **Lunch** including Networking and Intellectual Challenges Discussion
13:30 **"Safe and General Energy-Aware Programming with Disciplined Approximation"** - Luis Ceze, University of Washington
14:30 **Discussion** followed by a short Coffee Break
15:15 **"Link-Time Optimization for Instruction Cache Power Efficiency"**
Tim Jones, University of Cambridge
16:00 **"System-Level Energy Modelling"**
Geza Lore, ARM Holdings Ltd.
"Creating Energy Efficient Software for Multi-Threaded, Multi-Core Processors"
Steve Kerrison, University of Bristol
∼16:45 **Discussion and Conclusion from Day 1**
17:30 **Wine Reception** and Networking
18:00 **END** of formal part Day 1

Thursday, 14th July 2011

8:30 **Registration** and Coffee
9:00 **"Energy-Efficient Embedded Computing"**
Peter Marwedel, TU Dortmund
10:00 **Discussion** followed by a short Coffee Break
10:30 **Bring your WILD & CRAZY ideas (WACI) - Brainstorming Session**
∼12:00 **What next?**
Small Group Discussions of Intellectual Challenges and how to take these forward
13:00 **Lunch** including Networking and Carrying on the **What next?** Discussion
14:00 **END of formal part**
14:15 **Room 0.01 remains available** for informal discussions and brainstorming
17:00 **CLOSE**, Room 0.01 will be locked

[1]Supported by the Institute for Advanced Studies (`http://www.bris.ac.uk/ias`), the Merchant Venturers School of Engineering and Cadence Design Systems.

Abstracts

Luis Ceze, University of Washington, US
"Safe and General Energy-Aware Programming with Disciplined Approximation"

Abstract: Energy is increasingly a first-order concern in computer systems. Exploiting energy-accuracy trade-offs is an attractive choice in applications that can tolerate inaccuracies. Recent work has explored exposing this trade-off in programming models. A key challenge, though, is how to isolate parts of the program that must be precise from those that can be approximated so that a program functions correctly even as quality of service degrades.

We propose using type qualifiers to declare data that may be subject to approximate computation. Using these types, the system automatically maps approximate variables to low-power storage, uses low-power operations, and even applies more energy-efficient algorithms provided by the programmer. In addition, the system can statically guarantee isolation of the precise program component from the approximate component. This allows a programmer to control explicitly how information flows from approximate data to precise data. Importantly, employing static analysis eliminates the need for dynamic checks, further improving energy savings. As a proof of concept, we develop EnerJ, an extension to Java that adds approximate data types. We also propose a hardware architecture that offers explicit approximate storage and computation. We port several applications to EnerJ and show that our extensions are expressive and effective; a small number of annotations lead to significant potential energy savings (10% - 50%) at very little accuracy cost. This talk will conclude with an overview of our current/future research directions in hardware support for disciplined approximation.

Luis Ceze is an Assistant Professor in the Computer Science and Engineering Department at the University of Washington. His research focuses on computer architecture, programming languages and OS to improve the programmability, reliability and energy efficiency of multiprocessor systems. He has co-authored over 40 papers in these areas, and had several papers selected as IEEE Micro Top Picks and CACM research Highlights. He participated in the Blue Gene, Cyclops, and PERCS projects at IBM Research and is a recipient of several IBM awards. He is also a recipient of an NSF CAREER Award, a Sloan Research Fellowship and a Microsoft Research Faculty Fellowship. He co-founded Corensic, a UW-CSE spin-off company, where he is a part-time consultant.

Tim Jones, University of Cambridge, UK
"Link-Time Optimization for Instruction Cache Power Efficiency"

Abstract: The instruction cache is a critical component in any microprocessor which must have high performance to enable fetching of instructions on every cycle. However, current designs waste a large amount of energy on each access as tags and data banks from all cache ways are consulted in parallel to fetch the correct instructions as quickly as possible. Existing approaches to reduce this overhead remove unnecessary accesses to the data banks or to the ways that are not likely to hit. However, tag banks still need to be checked, which wastes power if you know exactly where the required instructions are in the cache.

This talk presents a new hybrid hardware and linker-assisted approach to tagless instruction caching. Our novel cache architecture, supported by the compilation toolchain, removes the need for tag checks entirely for the majority of cache accesses. The linker places frequently-executed instructions in specific program regions that are then mapped into the cache without the need for tag checks. This requires minor hardware modifications, no ISA changes and works across cache configurations. Our approach keeps the software and hardware independent, resulting in both backward and forward compatibility.

Evaluation on a superscalar processor with and without SMT support shows power savings of 66% within the instruction cache with no loss of performance. This translates to a 49% saving when considering the combined power of the instruction cache and translation lookaside buffer, which is involved in managing our tagless scheme.

Dr. Timothy M. Jones is a Royal Academy of Engineering / EPSRC Research Fellow at the University of Cambridge where he is investigating compiler-directed schemes for processor power saving. He spent the whole of 2010 working at Harvard with Professor David Brooks and his research team on compiler support for processor reliability. He also has interests in automatic parallelisation and the incorporation of machine learning into compiler optimisation and microarchitectural design. Dr. Jones holds a PhD from the University of Edinburgh and an MEng from the University of Bristol.

Geza Lore, ARM Holdings Ltd., UK
"System-Level Energy Modelling"

Abstract: System power and energy optimisation is a complex problem due to the interactions between different components. Focusing on a component or behaviour in isolation can lead to suboptimal designs, and a system-level methodology is needed. This presentation introduces a methodology used in ARM that enables the construction of high level power and energy models for system building blocks. These models enable the power analysis of complete systems running complex applications using emulation hardware or high level simulation, thus opening up the opportunity to make informed Power-Performance tradeoffs about system architecture, evaluation of system level power control solutions and identifying energy bottlenecks.

Geza Lore is an engineer in the systems research group of ARM Ltd. His research interests include high-performance, energy efficient computer systems, with a focus on memory and communication system architecture. Lore received an MSc in Electrical Engineering from the Budapest University of Technology and Economics. Contact him at: Geza.Lore@arm.com

Steve Kerrison, University of Bristol, UK
"Creating Energy Efficient Software for Multi-Threaded, Multi-Core Processors"

Abstract: Truly effective energy efficient computing requires a synergy between hardware capabilities, control hooks and software behaviour. Delivering this requires us to re-think our hardware implementations, our programming model and our overall approach to hardware/software co-design. In this talk we explore the challenges of modelling and optimising software energy consumption in a hardware multi-threaded architecture - the XMOS XCore. We examine how existing energy modelling techniques must be adapted to handle such parallel architectures and propose new techniques for energy-optimisation that could change the way we think about programming for energy efficiency.

Steve Kerrison received his M.Eng. from the University of Bristol. He is now part of the university's Micro-electronics Research Group. The group comprises researchers and staff from both the Computer Science and Electronics & Electrical Engineering departments. Current areas of research include High Performance Computing, Verification and Energy Aware Computing.

Steve's focus is on energy aware software development and optimisation, particularly in embedded systems. He is working to improve the system development work-flow to make energy awareness a 1st class citizen and to streamline the process of enhancing energy efficiency at the software level. Over the past year he has been working with XMOS, exploring opportunities for software-level energy enhancements in multi-threaded processor architectures.

Peter Marwedel, TU Dortmund, Germany

"Energy-Efficient Embedded Computing"

Abstract: For mobile embedded systems, only very limited amounts of electrical energy are available. At the same time, there is a trend toward higher performance also for mobile systems. As a result, the potential for energy-efficient computing must be fully exploited for such systems. Therefore, energy-efficient hardware design as well as energy-efficient hardware/software interfaces must be used. This talk focuses on the latter.

We will start with a look at the memory hierarchy and we will demonstrate how scratchpad memories can be used for implementing fast, energy-efficient and timing-predictable memory accesses. We will provide an overview of memory allocation techniques for scratchpad memories. Next, we will look at processors. An energy model for ARM-based processors will be presented. Looking at entire systems, we will also demonstrate how graphics processors can be used for energy-efficient image analysis. Finally, we will provide an outlook on research on energy-efficiency within the collaborative research project SFB 876. This project focuses on resource-efficient machine learning and covers areas at the system level (see www.sfb876.tu-dortmund.de).

Dr. Peter Marwedel studied physics at the University of Kiel, Germany. He received his PhD in that subject in 1974. As a post-doc, he published some of the first papers on high-level synthesis and retargetable compilation in the context of the MIMOLA hardware description language. In 1987, his habilitation thesis in computer science (a thesis required for becoming a professor) was accepted. Since 1989, he is holding a chair for computer engineering and embedded systems at the Computer Science Department of TU Dortmund. He is also chairing ICD, a local spin-off of TU Dortmund. His research interests include design automation for embedded systems, in particular the generation of efficient embedded software. Focus is on energy efficiency and timing predictability. Since 2001, Dr. Marwedel published papers on energy-efficient software and compiler-supported use of scratchpad memories. He is the author of one of the few textbooks on embedded systems. Since 2011, he is the vice-chair of the collaborative research center SFB 876, aiming at resource-efficient analysis of large data sets. Dr. Marwedel is an IEEE Fellow.